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Remarks

The Examiner has yet to indicate whether the drawings of the application are acceptable. It is respectfully requested that the Notice of Draftsperson's Patent Drawing Review (PTO-948) be provided.

Claims 9, 12, 32 and 35 are cancelled, without prejudice, by this amendment. Claims 1-8, 10, 11, 13-16, 31, 33, 34, 36, 37, and 40 have been amended. Support for the amended claims is provided for in the specification and drawing figures; no new matter has been entered. Therefore, claims 1-8, 10, 11, 13-16, 21-28, 31, 33, 34, 36-40 are pending in this application.

35 U.S.C. § 103

Claims 1-3, 6-11, 13-16 and 21-26, 31, 33, 36, and 38-40 are rejected under 35 USC 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Kizilyalli et al (US 6,174,807), and Shibata ('679) or Liu ('124).

In the Office Action, the Examiner agrees that the combination of AAPA and Kizilyalli et al fails to teach or suggest the limitation of an oxide diffusion barrier layer as recited by the claims. To cure this deficiency, the Examiner points to Shibata or Liu for teaching an oxide layer interposed between a polysilicon layer and metalized layer.

Applicants wish to point out that Kizilyalli et al disclose that the p+ gate dopant barrier 50 is preferably comprised of nitrogen implanted into and concentrated near the surface of the polysilicon layer 20 above the p-tub region 24. See FIG. 3 and column 3, lines 5-10. Kizilyalli et al also suggest that an argon-rich region may also be a suitable barrier. Id., line 1. Accordingly, Kizilyalli does not suggest replacing the nitrogen region or argon-rich region with an oxide region. For apparent reasons, the AAPA is also silent on such a suggestion. Liu only mentions that an oxide layer has been used, but teaches away from using the oxide layer as a barrier layer by pointing out the problems with the Tsukamoto et al. process. Shibata also fails to suggest that the oxide layer may be used

as a substitute to either a nitrogen region or argon-rich region. Accordingly, there is no motivation provided by the references to be combined in the manner suggested by the Examiner.

In order to establish a *prima facie* case of obviousness, the Examiner has the burden of proving, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the reference itself or in the knowledge available in the art, to modify that reference's teachings; 2) there is a reasonable expectation on the part of the skilled practitioner that the modification or combination has a reasonable expectation of success; and 3) the prior art reference must teach or suggest all of the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Both the teaching or suggestion and the reasonable expectation of success must be found in the prior art and not based on an applicant's disclosure. *Id.*

In carrying this burden, the Examiner "must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious." *Ex parte Clapp*, 227 USPQ 972, 973 (PTOBPAI 1985). A rejection based on §103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. *In re Warner*, 154 USPQ 173, 178 (CCPA 1967). The Examiner may *not*, because he may doubt that the invention is patentable, resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in his required factual basis. *Id.*

However, in an effort to further prosecution of this application, independent claims 1-8, 10, 11, 13-16, 31 and 40 have been amended to recite that the oxide layer extends only over a portion of the isolation region. Additionally, please note that independent claims 1-8, 10, 11, 13-16, 31 and 40 also recite that the gate electrode structure has a N+ polysilicon layer and a P+ polysilicon layer. The same structure is neither disclosed nor suggested by the suggested combination of references.

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Applicants note that the oxide layer 8 of Shibata extends completely over the channel region separating the LLD regions 6, and that no portion of the oxide layer extends over an isolation region as is recited by the amended claims. Additionally, as Shibata is concerned with alleviating the deterioration inherent in an LDD structure of a conventional MOFET, polysilicon layer 3 of Shibata does not is not having a N+ polysilicon layer and a P+ polysilicon layer as also recited by the claims.

Liu discloses as prior art growing an oxide layer between a tungsten silicide and polysilicon layers in W-polycide dual gate and buried metal on diffusion layer structures for DRAM-embedded logic devices. There is no suggestion provided in Liu that this oxide layer is provided over only a portion of the isolation region as recited by the amended independent claims 1-16, 31, and 40. In fact, Liu is completely silent on the location of the isolation region and its relationship to the oxide layer. Furthermore, Liu states that a lateral diffusion problem remains with the Tsukamoto et al. process. Col. 2, lines 56-59. This implies that the oxide layer in the Tsukamoto et al. process completely covers the polysilicon layer, and hence most likely the isolation region as is also shown by Liu in FIGS. 1-4.

Accordingly, the teachings of Shibata and Liu suggest to one skilled in the art forming an oxide layer on the entire polysilicon layer. Combining the teachings of the AAPA and Kizilyalli et al. in view of Shibata or Liu (even though no such motivation is provided) results in replacing the nitrogen region or argon region with an oxide layer that extends over the entire polysilicon layer, thereby extending the oxide layer fully over the entire isolation region. Thus, such as combinations of references would fail to produce the recited invention of the amended claims.

Claims 4, 5, 27, 34, and 37 are rejected as being unpatentable over AAPA in combination with Kizilyalli et al and Shibata or Liu as applied to claims 1-3, 6-11, 13-16, 21-26, 31, 33 ,36, and 38-40 and further in view of Fuji et al (US 5,355,010). Fuji et al is cited for disclosing a CMOS structure, and therefore the suggested combination of claim

for same reason noted above does not disclosed the structure of amended independent claims 4 and 5. As claims 27, 34 and 37 depend from amended and unobvious independent claims, these claims are also believed allowable.

Claims 1-3, 6, 9-16, 21-26, and 31-40 are rejected as being unpatentable over AAPA in combination with Hunter et al (US 5,940,725), and Shibata or Liu. Hunter et al disclose a silicon-rich nitride diffusion barrier layer 48 provided completely over the isolation region 34 (FIGS. 2B-D) and not at all after completing the step illustrated by FIG. 2E. Accordingly, in addition to the reason noted above, the AAPA in combination with Hunter et al, and Shibata or Liu fail to teach or suggest the limitations of an oxide diffusion barrier layer formed in the polysilicide gate electrode structure and over only a portion of the isolation region, as recited by amended claims.

Double Patenting

Claim 40 has been amended to further avoid a substantial duplication of pending claims 1-8, 10, 11, and 13-16.

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Conclusion

Applicants respectfully submit that, in view of the above amendments and remarks the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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